**Detailed proposal**

1. **\* Please provide details of your proposed research to include (a) aims, objectives and central research questions of the project, (b) how existing literature on the topic has been used to inform the proposal and (c) how the project will advance state of the art and make a contribution to existing knowledge: 500 words**

(a) Aims, Objectives, and Central Research Questions:

The primary goal of this research is to optimize the Network-on-Chip (NoC) architecture in AI accelerators, particularly focusing on AMD’s VERSAL platform, to improve the performance of Multi-Processor System-on-Chip (MPSoC) and ultimately enhance streaming media performance. Given the high bandwidth and low latency requirements of multimedia streaming, optimizing NoC within MPSoC systems is crucial.

The objectives are to develop tools and methodologies to:

1. Benchmark the NoC interconnect to identify performance bottlenecks in media streaming within MPSoC systems.

2. Determine optimal NoC configuration parameters to minimize latency and maximize throughput for multimedia data processing across multiple cores.

3. Perform an energy-performance trade-off analysis for streaming applications to optimize speed and power consumption in MPSoC environments.

4. Investigate optimizations in data transfer formats and precision across processing units while maintaining streaming quality and AI model accuracy.

The central research questions are:

1. How can NoC configuration in VERSAL AI accelerators be optimized to reduce latency and improve throughput in media streaming tasks within MPSoC systems?

2. What are the performance-energy trade-offs in different NoC configurations for MPSoC, particularly for streaming applications?

3. How can data representation formats be optimized to improve energy efficiency without compromising streaming quality or AI model accuracy?

(b) Existing Literature and Its Influence on the Proposal:

Current literature shows that NoC optimization is critical for improving media streaming performance in AI accelerators, particularly within MPSoC environments. Studies on VERSAL AI engines and packet switching have highlighted the challenges of managing data transfers in high-bandwidth, low-latency environments like streaming. However, existing research often lacks user-driven tools capable of optimizing NoC for multi-core streaming workloads in MPSoC. Research on energy efficiency in large-scale AI models, especially in high-resolution media processing, further underscores the importance of hardware-level optimizations in MPSoC systems. This proposal builds on these findings to develop practical tools that address NoC configuration complexities, focusing on real-time streaming applications within MPSoC platforms.

(c) Advancing the State of the Art and Contribution to Knowledge:

This project advances the state of the art by offering a framework for optimizing NoC in AI accelerators, specifically improving MPSoC performance for streaming media applications. Unlike existing tools that focus primarily on task mapping, this research will focus on fine-tuning NoC configurations for better performance, energy efficiency, and scalability in streaming applications. By analyzing NoC configurations, energy-performance trade-offs, and data transfer optimizations, the project contributes new methods for handling complex workloads in MPSoC systems. Collaboration with AMD’s Versal research team will provide real-world validation, ensuring that the research outcomes are both practical and impactful. Ultimately, this research delivers scalable solutions for enhancing hardware performance in MPSoC systems, addressing the high demands of streaming media in terms of bandwidth, latency, and energy efficiency.

1. **\* Please detail the research design and methodologies to be employed in carrying out your scholarship which should be described in sufficient detail to demonstrate your thorough understanding of the research topic: 500 words**

This research follows a multi-phase approach to optimize NoC architecture in **AMD’s VERSAL AI accelerators for MPSoC systems**, with a particular focus on **streaming applications**. The design is centered around sustainability by benchmarking state-of-the-art implementations and maximizing the reuse of components.

**Benchmarking the State-of-the-Art (SOTA) and Analysis**:  
In this phase, we will benchmark existing NoC implementations on AMD’s VERSAL platform using custom profiling scripts. Key metrics such as latency, congestion points, and bandwidth limitations will be evaluated under AI streaming workloads in an MPSoC environment. By benchmarking against current SOTA designs, we will identify performance bottlenecks and gaps, providing critical insights into how NoC configurations affect streaming applications within MPSoC systems. This analysis will guide targeted optimizations.

**Optimization of NoC Configuration Parameters**:  
Using tools like BookSim2 and AMD’s NoC modeling software, we will optimize **NoC configuration parameters** such as routing algorithms, buffer sizes, and link widths. This phase aims to reduce latency and maximize throughput for MPSoC-based streaming applications. We will leverage **genetic algorithms** and other automated search methods to efficiently explore the design space. The optimization process will prioritize sustainability by reusing existing components, ensuring that NoC enhancements are seamlessly integrated with minimal changes to current systems.

**Energy-Aware Task Scheduling**:  
Building on energy-efficient scheduling methods, we will implement **Dynamic Voltage and Frequency Scaling (DVFS)** to optimize energy consumption. Task scheduling will balance workloads across multiple MPSoC cores, ensuring resource efficiency while adhering to system memory constraints. These optimizations will reduce power consumption and latency, tailored specifically for **streaming applications** where sustained data transfer and low latency are crucial.

**Domain-Specific Energy-Performance Trade-off Analysis**:  
We will conduct an in-depth **energy-performance analysis** using AMD’s VERSAL toolkit, focusing on the balance between performance and energy consumption in streaming applications. This phase will evaluate how NoC configurations and DVFS contribute to real-time energy efficiency. The goal is to optimize energy use while maintaining high throughput, ensuring relevance for MPSoC-based streaming applications.

**Low-level Data Transfer Optimization**:  
This phase will explore **custom data encoding, compression techniques, and precision management**, specifically designed to reduce data size and bandwidth usage across the NoC. These optimizations will ensure efficient bandwidth use without compromising AI model accuracy or performance in **real-time streaming** tasks.

**Validation in the Application Domain**:  
The final phase will validate the proposed NoC optimizations in **real-world MPSoC streaming applications**, using AMD’s VERSAL hardware. We will test the system against existing interfaces to demonstrate seamless integration with minimal modifications, reinforcing sustainability objectives. Key performance metrics such as frames per second, energy per inference, and bandwidth efficiency will be measured. The goal is to validate that the NoC optimizations provide significant performance gains while maximizing component reuse and energy efficiency in streaming environments.

1. **\* Please provide a schedule to include (a) milestones and deliverables for completion of the proposed research, (b) risks that might endanger reaching these deliverables and (c) the contingency plans to be put in place in order to mitigate these risks: 500 words**

Year 1: Foundation and Setup

The first year will focus on establishing a robust foundation. The first quarter will involve an in-depth literature review on NoC architecture within MPSoC systems, AMD VERSAL platforms, and the requirements for streaming applications, resulting in a report identifying research gaps, particularly in the context of streaming and sustainability. By the second quarter, the research environment, including AMD VERSAL development kits and simulation tools like BookSim2, will be set up. The third quarter will benchmark the VERSAL NoC under AI streaming workloads, producing a baseline performance report. In the final quarter, initial NoC optimization models for MPSoC streaming applications will be developed.

Risks: Delays in hardware access.

Mitigation: Use alternative simulation tools and maintain collaboration with AMD.

Year 2: Exploration and Optimization

In Year 2, the focus will shift to exploring NoC configurations and developing optimization algorithms. In the first half, simulation tools will be used to explore routing algorithms, buffer sizes, and other NoC parameters, leading to a detailed analysis. The third quarter will focus on developing optimization algorithms to enhance NoC performance and energy efficiency for MPSoC streaming applications. In the fourth quarter, an energy-performance trade-off analysis will begin, resulting in an interim report.

Risks: Algorithm failure or insufficient computational resources.

Mitigation: Iteratively refine algorithms and seek additional computational resources through cloud services or institutional support.

Year 3: Data Transfer Optimization and Validation

In Year 3, the focus will be on low-level data transfer optimizations and validation. The first two quarters will involve optimizing data encoding and compression techniques to reduce bandwidth usage for real-time NoC transfers in MPSoC systems. The third quarter will integrate optimized NoC configurations into a unified framework, and the fourth quarter will validate these configurations on AMD’s VERSAL hardware, measuring performance metrics such as frames per second, energy consumption, and bandwidth efficiency.

Risks: Hardware limitations or insufficient performance improvements.

Mitigation: Collaborate with AMD for troubleshooting and iterative tuning to address performance issues.

Year 4: Final Evaluation and Dissemination

Year 4 will focus on final evaluation and dissemination. The first two quarters will compare the optimized NoC performance to the baseline established in Year 1, focusing on streaming performance and sustainability. Findings will be documented in a performance evaluation report. The third quarter will focus on documenting energy efficiency improvements, and the final quarter will prepare the research for publication in academic journals and submission to conferences.

Risks: Delays in finalizing research or meeting publication standards.

Mitigation: Allocate buffer time to address unforeseen challenges and seek early feedback for refinement.

1. **\* Please describe any specialist knowledge or data required to undertake your proposed research, such as language competency, technical skills or use of specialist software. If this knowledge or data is not already in place, details should be provided as to how it will be acquired over the course of the scholarship:**

This research requires a combination of specialized knowledge, technical skills, and software tools to optimize the NoC architecture in AMD VERSAL AI accelerators, particularly within MPSoC systems for streaming media applications.

Technical Skills and Knowledge:

1. Network-on-Chip (NoC) Architecture:

A deep understanding of NoC design, including routing algorithms, buffer management, and data flow optimization within MPSoC systems, is essential. I have a strong foundation in these areas and will further enhance my expertise through experimentation and literature focused on NoC optimization for real-time streaming tasks.

2. Deep Learning Accelerators and Hardware Design:

Expertise in deep learning accelerators, particularly the AMD VERSAL architecture, is crucial for optimizing NoC within MPSoC systems. My background in hardware design provides a solid base, and I will further develop this through direct engagement with VERSAL development kits, focusing on streaming application optimization.

3. Data Transfer and Encoding Techniques:

Understanding data encoding and compression techniques is key to optimizing NoC data movement, especially for real-time streaming tasks in MPSoC environments. While I am familiar with basic methods, I will deepen this knowledge through targeted experimentation and literature review on bandwidth-efficient streaming solutions.

Specialist Software and Tools:

1. Simulation Tools (e.g., BookSim, AMD NoC Modeling Software):

Proficiency in NoC simulation tools like BookSim and AMD’s NoC modeling software is essential for exploring and optimizing NoC configurations. I will gain expertise through tutorials and hands-on experimentation with these tools.

2. Programming Languages (Python, C++):

Strong programming skills in Python and C++ are required for algorithm development and simulation. My proficiency in these languages positions me to efficiently implement and test NoC configurations tailored for MPSoC systems and streaming applications.

3. Power Modeling and Profiling Tools:

Familiarity with AMD’s power modeling tools is crucial for conducting energy-performance trade-off analysis. I will develop proficiency by working within AMD’s development environment, focusing on energy-efficient solutions for MPSoC-based streaming applications.

Data and Access Requirements:

1. Access to AMD VERSAL Development Kits:

Access to AMD VERSAL development kits and the HPC platform HACC is crucial for validating NoC optimizations in real-world settings. These resources are secured through collaboration with AMD and ETH Zurich.

2. Literature and Documentation:

Ongoing access to the latest research papers and technical documentation is essential to stay current with industry advancements, guiding the direction of the NoC optimization efforts.

By building on my current skills and acquiring additional expertise through targeted learning, experimentation, and collaboration, I am well-prepared to undertake this research. This combination of specialized knowledge and access to necessary resources ensures the successful optimization of NoC for MPSoC systems, particularly for streaming media applications and sustainable design.

1. **\* Please outline your plans for the dissemination and knowledge exchange of your research, including publications, conference attendance, poster presentations, reports and outreach activities. Details should also be provided as to how the impact of your research will be measured:**

Publications:

The primary method of disseminating research results will be through publications in high-impact, peer-reviewed journals such as IEEE Transactions on Computers, ACM Transactions on Design Automation of Electronic Systems, and the Journal of Parallel and Distributed Computing. These journals cover key areas like computer architecture, AI hardware, energy-efficient design, and embedded systems, making them ideal for sharing insights related to NoC optimization for streaming media and sustainable design. The research will be published in phases, including initial findings on NoC benchmarking for streaming workloads, progress in NoC configuration optimization for real-time tasks, energy-performance trade-off analysis, and the development of a sustainable NoC framework for AI accelerators. Each paper will provide detailed methodology and results, contributing valuable insights to both academic and industrial communities.

Conference Attendance and Reporting:

Presenting at international conferences is a key element of the dissemination strategy. I plan to submit papers and present findings at conferences such as the IEEE/ACM International Networks-on-Chip Symposium (NoCS), the International Conference on Field-Programmable Logic and Applications (FPL), and Design Automation Conference (DAC). These conferences are ideal platforms for sharing research findings in NoC for AI streaming applications, as well as for exchanging knowledge with experts and industry professionals. Feedback received from these conferences will help refine the research, while fostering collaboration opportunities with peers in the field.

Poster Presentations and Workshops:

In addition to oral presentations, poster sessions at events such as the IEEE Symposium on High-Performance Computing Architecture (HPCA) will facilitate direct interaction with researchers. These platforms are crucial for sharing research on sustainable NoC designs for real-time multimedia applications. Participation in workshops focused on AI accelerators and hardware optimization will further disseminate the findings and foster in-depth discussions, while also exploring potential real-world applications.

Reporting and Industry Collaboration:

Regular progress reports will be shared with partners, particularly the AMD Versal research team, detailing methodology, findings, and insights from real-world applications of NoC optimizations. These reports will encourage ongoing collaboration, with the potential to influence future product designs. Internal seminars and webinars with industry partners will also be conducted, ensuring a sustainable and practical application of research outcomes in industry settings.

Outreach Activities:

To extend the research’s impact, outreach will include writing articles for technology blogs and contributing to open-access platforms. These efforts will simplify the research findings, making them accessible to a broader audience, including those interested in NoC optimization for streaming media applications. Workshops and lectures within academic institutions will also be organized to promote sustainable NoC designs in courses and academic projects, inspiring future research directions.

Impact Assessment:

Research impact will be measured by the quality and number of publications, citation counts, and the feedback received from conferences and industry collaborators, particularly AMD. The adoption of NoC optimization techniques for streaming media and sustainability in both academic and industrial settings will further gauge the research’s success. Additionally, outreach activities will be assessed through metrics such as blog post views, open-access downloads, and audience engagement, ensuring a broader societal impact.

1. **\* Please outline your reasons for choosing your proposed (a) academic supervisor(s) and (b) higher education institution making particular reference to how the chosen supervisor and institution**

I have selected Professor Shreejith Shanker as my academic supervisor due to his expertise in computer architecture, AI hardware acceleration, and NoC design. His involvement in projects focused on energy-efficient compute flows in the media industry aligns closely with my research on optimizing NoC for streaming applications. Additionally, Professor Shanker’s participation in a Horizon Europe (HEU) project investigating energy consumption in movie industry compute flows complements my focus on energy-performance trade-offs in real-time streaming tasks. His extensive experience with the AMD VERSAL architecture provides critical insights into optimizing NoC for real-time, energy-intensive applications. Furthermore, his established collaborations with industry partners like AMD ensure that my research will have practical relevance and access to cutting-edge resources. Under his supervision, I will receive guidance that integrates both academic rigor and industrial applications, essential for the success of my research.

Trinity College Dublin (TCD) offers an ideal environment for my research, known for its excellence in engineering, AI, and computer architecture. The School of Computer Science and Statistics provides access to state-of-the-art facilities, including AMD VERSAL platforms, which are essential for my NoC optimization efforts. TCD’s involvement in Horizon Europe projects related to sustainable computing in media applications aligns perfectly with my focus on energy-efficient NoC designs for streaming tasks. Moreover, TCD’s strong partnerships with industry leaders such as AMD will facilitate valuable collaboration, allowing my research to address both academic and practical challenges. TCD’s vibrant research community encourages innovation and societal impact, ensuring that my work contributes to the growing field of AI hardware optimization.

By selecting Professor Shreejith Shanker and Trinity College Dublin, I will benefit from exceptional mentorship, cutting-edge resources, and industry connections, all of which are crucial for advancing my research on NoC optimization for AI accelerators, particularly in the areas of streaming media and sustainable design. This combination of expertise and support will ensure my research makes a significant contribution to both academic knowledge and industrial practice.

1. **\* Please provide details of any proposed research trip(s) of more than four weeks duration which you believe will be necessary for the successful completion of your award:**

Proposed Local Research Trip

Location: AMD Research Lab, Dublin

Duration: 6 weeks

Objective: This research trip aims to collaborate directly with AMD's research team and gain hands-on access to the VERSAL hardware platform. Access to this hardware is critical for testing and validating the NoC optimization techniques developed in my research.

Reason for the Trip: While based at Trinity College Dublin, having extended access to AMD’s facilities will allow for hands-on experimentation with the VERSAL devices and enable real-time collaboration with AMD engineers. This direct engagement is essential for troubleshooting and fine-tuning NoC configurations, ensuring that the research meets industry standards and real-world requirements. The six-week period will allow uninterrupted access, facilitating comprehensive testing and validation of the proposed optimizations.

Expected Outcomes: During this six-week trip, I will conduct detailed experiments to measure key performance metrics such as latency, throughput, and energy efficiency on AMD’s VERSAL hardware. These results will be crucial in refining NoC optimization techniques and providing real-world validation for my research, ensuring the methods are both academically rigorous and industrially relevant.

Contribution to the Project: This research trip is a vital component of my project. It enables me to test the NoC optimizations directly on industry-grade hardware and receive immediate feedback from AMD engineers. This collaboration will ensure that the optimization techniques developed are not only theoretical but also practical and impactful for AI hardware optimization.

This local research trip will provide essential resources and expertise to guarantee the successful completion of my project.